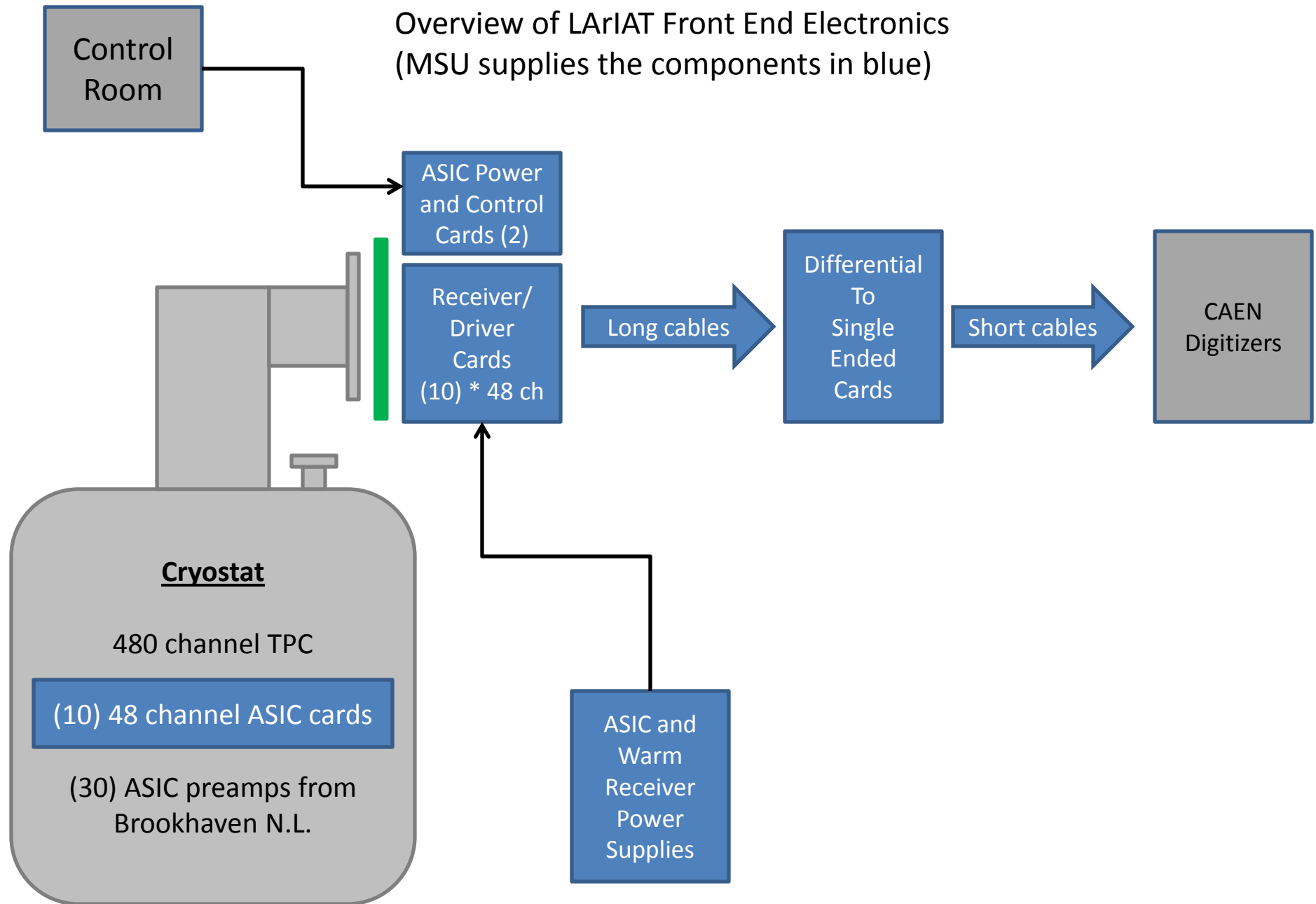


LArIAT Front End Electronics Update

May 20, 2014

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Overview of LArIAT Front End Electronics (MSU supplies the components in blue)



Front end card production

ASIC cards

Cards manufactured, now in assembly. Should be complete and at MSU by May 28. Next step: testing.

Cryostat feedthrough/backplane

Design is ongoing, expect to send for PCB production by May 26th.

We will verify design with Walter Jaskierny, etc. before production.

Expect a feedthrough card to be ready by June 9th Fermi visit.

Card should be leak-tested (Walter's suggestion).

Warm receiver/Driver cards

Design is overlapping with the feedthrough/backplane card design.

Expect cards to be ready by end of June.

Differential-to-single ended cards (close to CAEN digitizers)

Design not started yet.

Expect ~ 5 week turnaround from design start to finished cards.

ASIC Power and Control

We will make a working prototype soon (needed for testing).

A more refined version of the APC card is planned.

Cabling

Inside cryostat

Solid core FEP insulated ribbon cable. Will order cable + connectors soon.

Warm receiver to D2S (long cable run from cryostat to the CAEN digitizer rack)

The current plan is to go with Twist-and-Flat ribbon cable and standard headers (simple, fast).

(Still could consider the old ArgoNeuT cables, but they are probably too short at 25 feet).

D2S to CAEN digitizers

Not started yet. We can make or buy these cables.

Connection of Bias Voltages to the TPC

In ArgoNeuT, Bo, and Long-Bo we had filtering of the bias voltages inside the cryostat very close to the TPC.

The LArIAT wire planes are set up for either direct connection to bias voltage or for installation of a BV filtering card.

We will discuss this soon with Mitch Soderberg, etc.

Control of Front End ASICs from the LArIAT Control Room

The ASIC chips are controlled by a serial bit stream sent from the ASIC Power and Configuration (APC) card.

The current control plan is to have a local microcontroller on the APC card.

This microcontroller will communicate with the control room (RS485, optical, etc. → several possibilities).

We will set this up such that the microcontroller can be powered off during data acquisition (it's a potential noise source).

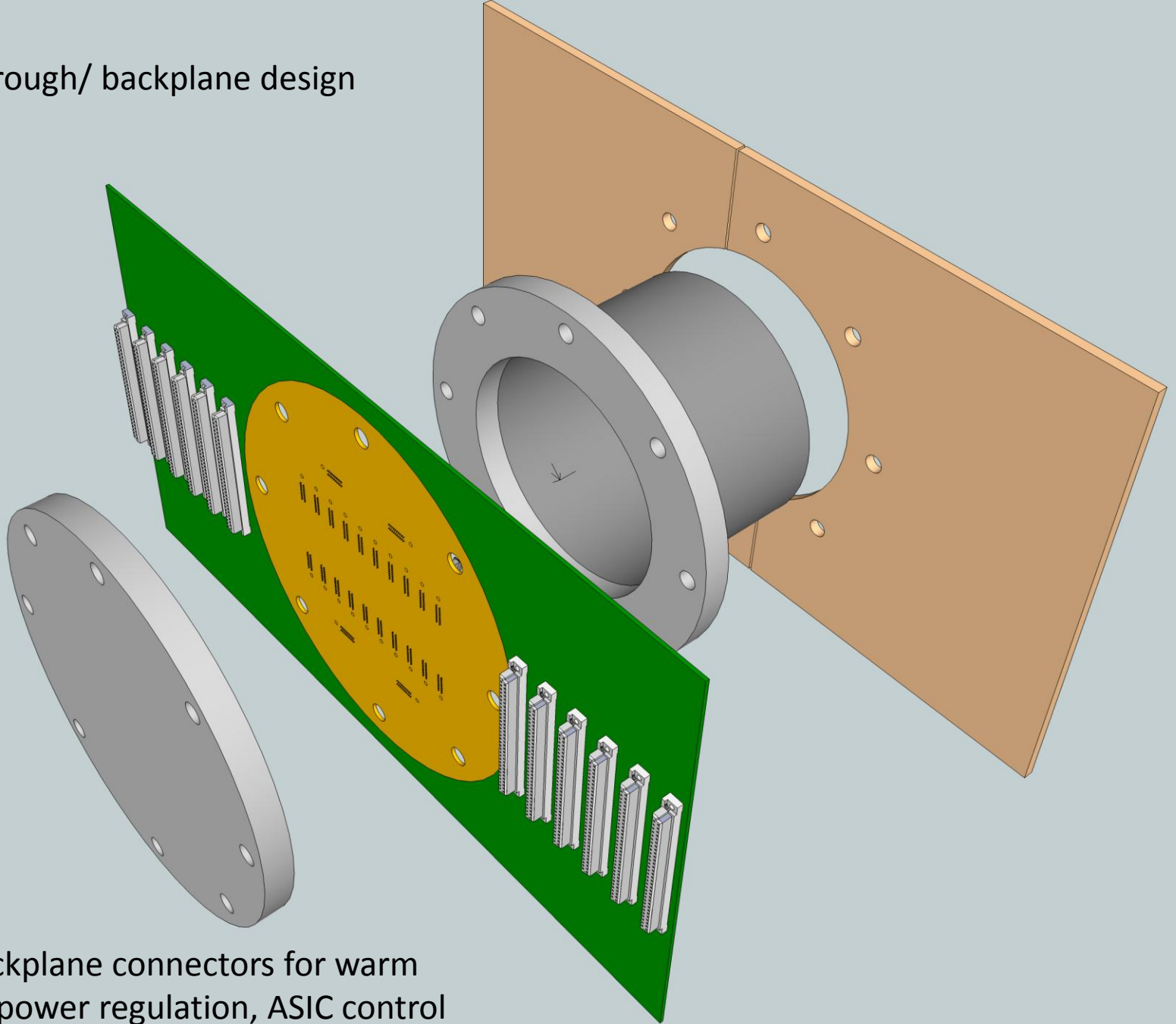
We need to discuss and outline the details of the interface to the Control Room sometime soon (with Bill Badgett, etc).

Documentation

We will provide the documents for the Fermilab Operational Readiness Review and also the Electrical Safety Review.

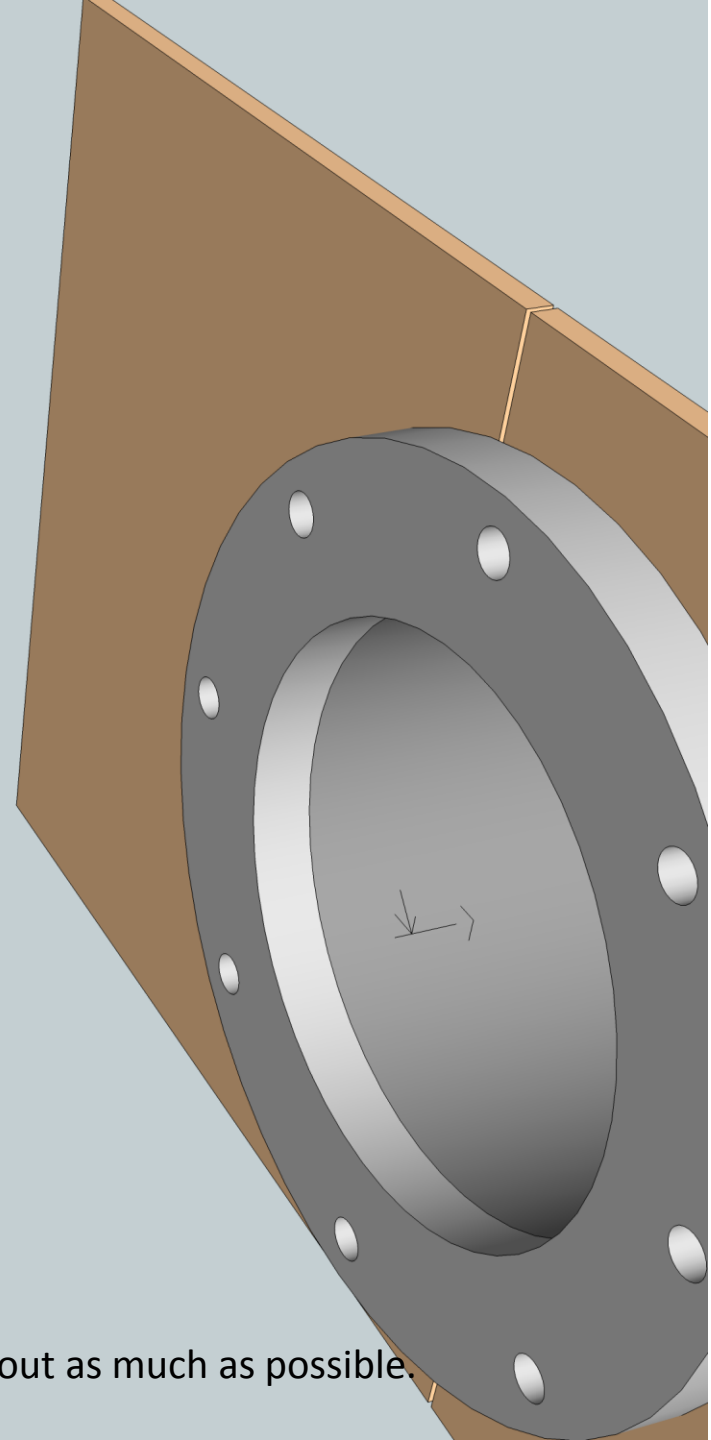
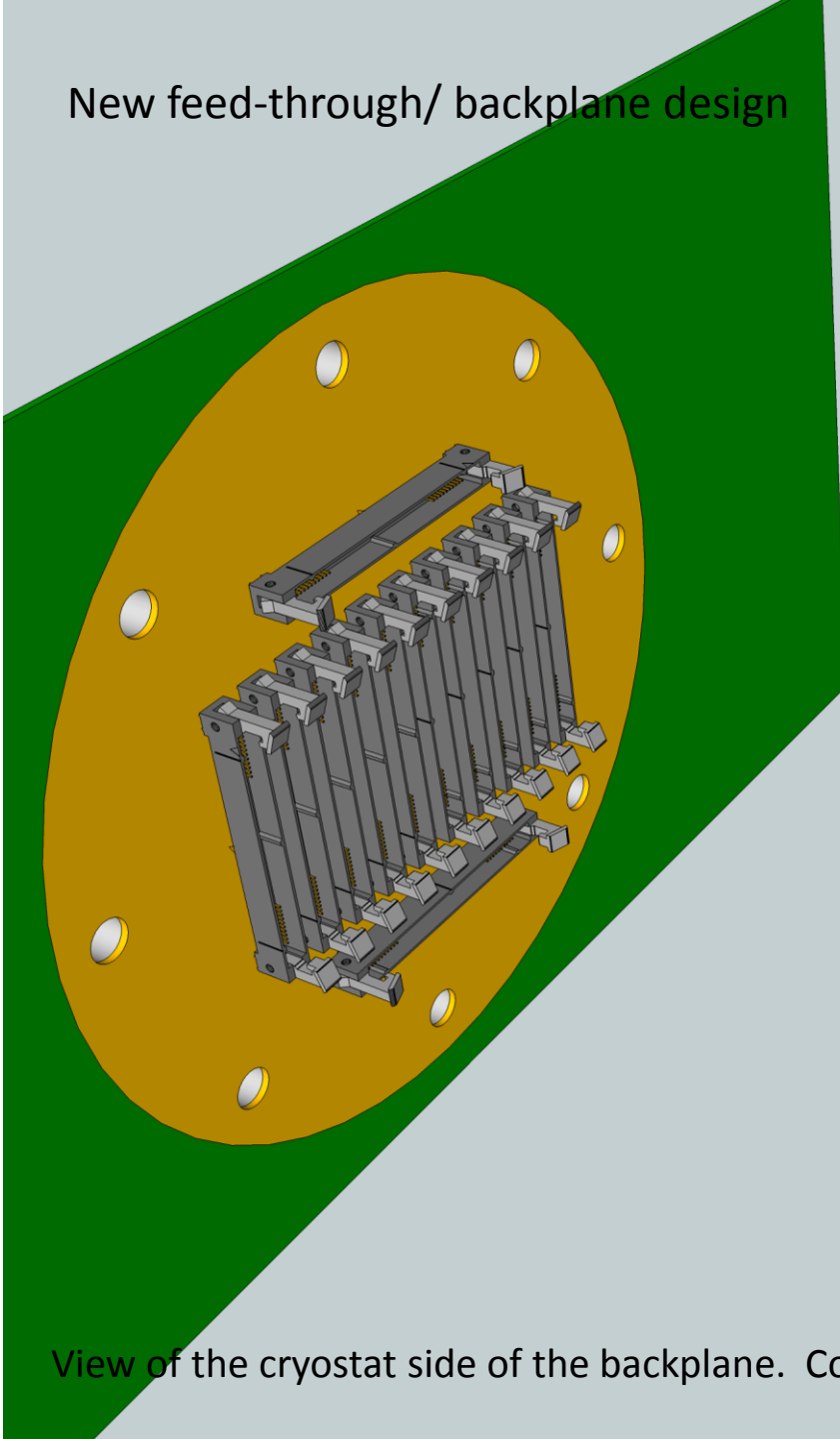
Backup slides

New feed-through/ backplane design



Design with backplane connectors for warm receivers, ASIC power regulation, ASIC control

New feed-through/ backplane design



View of the cryostat side of the backplane. Connectors are spread out as much as possible.